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WEST Search History

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	DB=	USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ	
	L13	L12 and @pd > 20030418	0
	L12	('6189128' 'JP401321562A' 'JP402059679A' '5812561') [ABPN1,NRPN,PN,TBAN,WKU]	6
	L11	L10 and scan\$4 same (test\$3 or debug\$4 or verif\$7 or diagno\$5) same (fan\$1in or fan\$1out) same (ic or (integrat\$3 near2 circuit\$3) or semi\$1conduct\$7 or memor\$7) same flip\$1flop same (program\$7 or adjust\$6 or vari\$4 or vary\$4 or configur\$7 or re\$1 configur\$7 or re\$1defin\$6)	0
	L10	L9 and scan\$4 same (test\$3 or debug\$4 or verif\$7 or diagno\$5) same (fan\$1in or fan\$1out) same (ic or (integrat\$3 near2 circuit\$3) or semi\$1conduct\$7 or memor\$7) same flip\$1flop	4
	L9	scan\$4 same (test\$3 or debug\$4 or verif\$7 or diagno\$5) same (fan\$1in or fan\$1out)	91
I	L8	L7 and @pd > 20030418	5
П	L7	L6 and scan\$4 with (test\$3 or debug\$4 or verif\$7 or diagno\$5) same (number or count\$3 or fan\$1in or fan\$1out) same (ic or (integrat\$3 near2 circuit\$3) or semi\$1conduct\$7 or memor\$7) same flip\$1flop same (program\$7 or adjust\$6 or vari\$4 or vary\$4 or configur\$7 or re\$1 configur\$7 or re\$1defin\$6) same (vector or pattern or sequence)	11
	L6	L5 and scan\$4 with (test\$3 or debug\$4 or verif\$7 or diagno\$5) same (number or count\$3 or fan\$1in or fan\$1out) same (ic or (integrat\$3 near2 circuit\$3) or semi\$1conduct\$7 or memor\$7) same flip\$1flop same (program\$7 or adjust\$6 or vari\$4 or vary\$4 or configur\$7 or re\$1 configur\$7 or re\$1defin\$6)	27
П	L5	scan\$4 same (test\$3 or debug\$4 or verif\$7 or diagno\$5) same (number or count\$3 or fan\$1in or fan\$1out) same (ic or (integrat\$3 near2 circuit\$3) or semi\$1conduct\$7 or memor\$7) same flip\$1flop same (program\$7 or adjust\$6 or vari\$4 or vary\$4 or configur\$7 or re\$1 configur\$7 or re\$1defin\$6)	52
	L4	('6189128' 'JP401321562A' 'JP402059679A' '5812561') [ABPN1,NRPN,PN,TBAN,WKU]	6
	L3	L2 and scan\$4 same (test\$3 or debug\$4 or verif\$7 or diagno\$5) same (fan\$1in or fan\$1out) same (ic or (integrat\$3 near2 circuit\$3) or semi\$1conduct\$7 or memor\$7) same flip\$1flop same (program\$7 or adjust\$6 or vari\$4 or vary\$4 or configur\$7 or re\$1 configur\$7 or re\$1defin\$6)	0
	L2	L1 and scan\$4 same (test\$3 or debug\$4 or verif\$7 or diagno\$5) same (fan\$1in or fan\$1out) same (ic or (integrat\$3 near2 circuit\$3) or semi\$1conduct\$7 or memor\$7) same flip\$1flop	4
m	L1	scan\$4 same (test\$3 or debug\$4 or verif\$7 or diagno\$5) same (fan\$1in or fan\$1out)	91

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END OF SEARCH HISTORY